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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,123	08/18/2003	Frank Yauchee Hui	Huang 4-5/075903-222	3499

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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,123	HUI ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9 December 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Dunn et al. (USPN 6,463,570 B1).

3. In reference to claims 1, 2, and 7, Dunn et al. (USPN 6,463,570 B1, hereinafter referred to as the "Dunn" reference) discloses a similar method. Figure 1B of Dunn discloses a frequency marker device (a ring oscillator) which is to be used on each die. Figures 3A and 3B of Dunn discloses that power is applied to the frequency marker device, the frequency of the frequency marker device is determined, and this frequency is associated with the integrated circuit device.

4. With regard to claims 3 and 4, Dunn makes it clear that the devices are formed on a wafer and that the frequency may be associated with a particular wafer or wafer lot (column 6, lines 23-32).

5. In reference to claim 5, Dunn discloses that the frequency can be associated with process steps (column 6, lines 28-32).

6. In reference to claim 6, Dunn states that the frequency may be associated with the location of the die on the wafer (column 5, lines 47-49, column 6, lines 2-3, and claims 3, 10, and 17).

7. With regard to claim 8, Dunn makes it clear that the ring oscillator, in figure 2A, uses an odd numbered plurality of serially connected inverter elements and a feedback loop (column 4, lines 2-3).

8. In reference to claim 9, Dunn shows a binary logic inverter to be used as the inverter in a circuit schematic in figure 1A and its actual implemented form in figure 1B.

9. In reference to claim 10, Dunn discloses a similar method. Figure 1B of Dunn discloses a frequency marker device (a ring oscillator) which is to be used on each die. Figures 3a and 3B of Dunn discloses that power is applied to the frequency marker device, the frequency of the frequency marker device is determined, and this frequency is associated with the integrated circuit device. Dunn states that the frequency may be associated with the location of the die on the wafer (column 5, lines 47-49, column 6, lines 2-3, column 6, lines 28-32 and 65-66, and claims 3, 10, and 17).

10. In reference to claim 11, Dunn (USPN 6,463,570 B1) discloses a similar manufacturing method. Figure 1B of Dunn discloses a frequency marker device (a ring oscillator) which is to be used on each die of a wafer. Each die comprises a semiconductor device. Figures 3A and 3B of Dunn discloses that power is applied to the frequency marker device, the frequency of the frequency marker device is determined, and this frequency is associated with the integrated circuit device. Dunn

makes it clear that this frequency is associated with the die after singulation (column 6, lines 59-67 and column 7, lines 1-11).

11. With regard to claim 12, Dunn makes it clear that the devices are formed on a wafer and that the frequency may be associated with a particular wafer or wafer lot (column 6, lines 23-32).

12. In reference to claim 13, Dunn discloses that the frequency can be associated with process steps (column 6, lines 28-32).

13. In reference to claim 14, Dunn states that the frequency may be associated with the location of the die on the wafer (column 5, lines 47-49, column 6, lines 2-3, column 6, lines 28-32 and 65-66, and claims 3, 10, and 17).

14. With regard to claims 15-17, Dunn (USPN 6,463,570 B1) discloses a die which meets the claim. Figure 1B of Dunn discloses a frequency identifier (a ring oscillator) which is to be used on each die. Dunn states that the frequency may be associated with the location of the die on the wafer (column 5, lines 47-49, column 6, lines 2-3, column 6, lines 28-32 and 65-66, claims 3, 10, and 17).

15. In reference to claim 18, Dunn makes it clear that the ring oscillator, in figure 2A, uses an odd numbered plurality of serially connected inverter elements and a feedback loop supplying the an output signal of a last one of the serially connected inverters to an input of another one of the serially connected inverters (column 4, lines 2-3).

16. In reference to claim 19, Dunn discloses that the frequency can be associated with process steps (column 6, lines 28-32).

17. Claims 1-4, 7, 11, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Lovett (USPN 6,664,799 B2).

18. In reference to claims 1, 2, and 7, Lovett (USPN 6,664,799 B2) discloses a similar method. Figure 1 of Lovett discloses an integrated circuit device (a die, not numerically labeled) having a frequency marker device (7, the oscillator). Lovett discloses that power is applied to the frequency marker device, the frequency of the frequency marker device is determined, and this frequency is associated with the integrated circuit device (column 3, lines 5-15).

19. With regard to claims 3 and 4, Lovett makes it clear that the devices are formed on a wafer and that the frequency may be associated with a particular wafer or wafer lot (column 3, lines 15-23).

20. In reference to claims 11 and 12, Lovett (USPN 6,664,799 B2) discloses a similar manufacturing method. Figure 1 of Lovett discloses an integrated circuit device (a die, not numerically labeled) having a frequency marker device (7, the oscillator). Each die comprises a semiconductor device. Lovett discloses that power is applied to the frequency marker device, the frequency of the frequency marker device is determined, and this frequency is associated with the integrated circuit device (column 3, lines 5-15). Lovett discloses that makes it clear that this frequency is associated with the die after singulation (column 3, lines 15-23).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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